

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Johan Sjöström et al.

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Title: **A Differential Transistor Pair**

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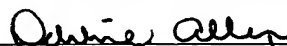
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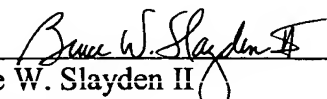
Dear Sir:

We enclose herewith a certified copy of Swedish patent application SE 0104116-9 which is the priority document for the above-referenced patent application.

Respectfully submitted,

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PATENT- OCH REGISTRERINGSVERKET
Patentavdelningen

Intyg Certificate

Härmed intygas att bifogade kopior överensstämmer med de handlingar som ursprungligen ingivits till Patent- och registreringsverket i nedannämnda ansökan.

This is to certify that the annexed is a true copy of the documents as originally filed with the Patent- and Registration Office in connection with the following patent application.



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Huvudföreläsning

A DIFFERENTIAL TRANSISTOR PAIR**TECHNICAL FIELD**

5 The invention relates generally to RF amplifiers and more specifically to a differential transistor pair.

BACKGROUND OF THE INVENTION

Power amplifiers using RF power transistors suffer from a reduction in gain with increasing frequency due to parasitic effects in the transistors. One of the most limiting
10 parasitic effects in large power transistors used at high frequencies is the so called "effective common-lead inductance", i.e. the magnetic coupling between the input and output loops of the transistor, causing inductive feedback. A number of techniques can be used to reduce that coupling. One can e.g. use substrate vias, a conductive substrate, or a large number of bond wires connected to ground. A differential amplifier is another
15 option, which also suppresses even harmonics, and has doubled input and output impedance levels.

Such power amplifiers are commonly built from two discrete transistors, in separate packages, or on separate dies in the same package, or one the same die but located in two
20 separate groups.

Fig. 1 is a schematic cross-sectional view of an embodiment of a known differential transistor pair.

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Two discrete LDMOS RF power transistors 1, 2 are located on a common package ground plane 3.

In a manner known per se, each transistor 1, 2 comprises in a substrate 4 and 5, respectively, a plurality of transistor cells C1, C2, each comprising a source region, a gate region, and a drain region.

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H. 11 11 11 11 11

Each such cell C1, C2 comprises a source region S, a gate region G and a drain region D as illustrated more in detail above the transistor 1 in Fig. 1. In a manner known per se, the source region S is connected to a substrate contact SC via a metal clamp C.

5 In each transistor 1, 2, all gate regions are coupled in parallel and connected to a common gate terminal (not illustrated). Moreover, all drain regions are coupled in parallel and connected to a common drain terminal (not illustrated) in each transistor 1, 2.

10 The source regions of the transistors 1, 2 are all interconnected via the heavily doped substrates 4, 5 and the ground plane 3.

In operation, RF current will flow from the gate region G and the drain region D of transistor 1 through the channel of transistor 1, through the source region S of transistor 1 and into the metal clamp C of transistor 1, through the substrate contact SC of transistor 15 1, through the substrate 4 of transistor 1, through the ground plane 3 and into the substrate 5 of transistor 2, through the substrate contact (not shown) of transistor 2, through the metal clamp (not shown) of transistor 2 and into the source region (not shown) of transistor 2, through the channel (not shown) of transistor 2 and into the gate region (not shown) and the drain region (not shown) of transistor 2 as indicated by line 6 20 in Fig. 1.

Since the effective impedance between the source regions of the transistors 1 and 2 is non-zero at RF and common to both input and output loops of the transistors, the gain will be reduced due to feedback in the known differential transistor pair.

25 SUMMARY OF THE INVENTION

The object of the invention is to bring about a differential transistor pair with a low effective impedance between the source regions of the transistors.

30 This is attained in that the differential transistor pair according to the invention comprises a plurality of transistor cells in a substrate. Each cell comprises first drain regions at the

respective edge of the cell, and a second drain region between the first drain regions. Source regions are provided between the respective first drain region and the second drain region. First gate regions are provided between the respective first drain region and the source regions, and second gate regions are provided between the source regions and the second drain region. The first drain regions of all cells are interconnected to a common first drain terminal. The second drain region of all cells are interconnected to a common second drain terminal. The first gate regions of all cells are interconnected to a common first gate terminal, and the second gate regions of all cells are interconnected to a common second gate terminal.

In the differential transistor pair according to the invention, RF currents will flow through the differential pair without passing through the bulk substrate.

BRIEF DESCRIPTION OF THE DRAWING

The invention will be described more in detail below with reference to the appended drawing on which Fig. 1, described above, is a schematic cross-sectional view of a known differential transistor pair, and Fig. 2 is a schematic cross-sectional view of an embodiment of a differential transistor pair in accordance with the invention.

DESCRIPTION OF THE INVENTION

Fig. 2 is a schematic cross-sectional view of an embodiment of a differential LDMOS transistor pair 7 in accordance with the invention.

In accordance with the invention, cells of two LDMOS transistors are merged two and two into a plurality of merged cells C3 in one and the same substrate 8 on a ground plane 9.

The merging can be accomplished by mirroring e.g. each transistor cell C1 in Fig. 1 at its source contact edge such that each combination of each transistor cell C1 and its mirrored version has a common substrate contact in the middle, sources on either side of the common substrate contact, interconnected via a common metal clamp, drains at the

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4

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edges, and gates in between. Each such combination of two cells is then mirrored at one drain edge such that each new combination of four cells has drains at the edges, a common drain in the middle, interconnected sources between the edge drains and the common drain, first gates between the edge drains and the interconnected sources, and second gates between the interconnected sources and the common drain.

In Fig. 2, an embodiment of such a merged cell C3 according to the invention is illustrated more in detail above the transistor pair 7.

- 10 The merged cell C3 comprises a drain region D11 at one edge of the cell and a drain region D12 at the other edge of the cell. The edge drain regions D11, D12 and all drain regions in the differential transistor pair 7 that correspond to those edge drain regions D11, D12 are interconnected to a common edge drain terminal VD1.
- 15 A central drain region D22 is located between the edge drain regions D11, D12. The central drain region D22 and all drain regions in the differential transistor pair 7 that correspond to that central drain region D22 are interconnected to a common central drain terminal VD2.
- 20 One common substrate contact SC11 with source regions S11 and S21 on either side interconnected via a common metal clamp C11 is located between the edge drain region D11 and the central drain region D22. Another common substrate contact SC12 with source regions S12 and S22 on either side interconnected via a common metal clamp C12 is located between the edge drain region D12 and the central drain region D22.
- 25 The common substrate contacts SC11, SC12 and all other substrate contacts in the differential transistor pair 7 that correspond to those substrate contacts SC11, SC12 are interconnected via the substrate 8 and the ground plane 9.
- 30 First gate regions G11, G12 are located between the edge drain regions D11, D12 and the common substrate contacts SC11, SC12. The first gate regions G11, G12 and all gate

regions in the differential transistor pair 7 that correspond to those first gate regions G11, G12 are interconnected to a common first gate terminal VG1.

5 Second gate regions G21, G22 are located between the common substrate contacts SC11, SC12 and the central drain region D22. The second gate regions G21, G22 and all gate regions in the differential transistor pair 7 that correspond to those second gate regions G21, G22 are interconnected to a common second gate terminal VG2.

10 In operation, RF currents will flow within the cells from the edge drain regions D11, D12 and the gate regions G11, G12 via the source regions S11, S12 into the common metal clamps C11, C12, through the source regions S21, S22 and to the central drain region D22 and the gate regions G21, G22 as indicated by lines 10 and 11 in Fig. 2.

15 Thus, RF currents will not flow through the substrate 8 and the ground plane 9.

Hereby, the source impedance of the differential pair according to the invention will be smaller and, consequently, the gain will be higher than in the known differential pair according to Fig. 1.

20 It is to be understood that the invention is not restricted to differential LDMOS transistor pairs but is equally applicable to bipolar junction transistors (BJTs). In a differential BJT pair (not shown), there would be collector regions that correspond to the drain regions in Fig. 2, emitter regions that correspond to the source regions in Fig. 2, and base regions that correspond to the gate regions in Fig. 2.

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Int. Patent application for

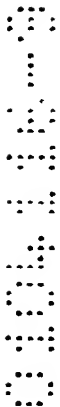
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CLAIM

A differential transistor pair, characterized in that it comprises a plurality of transistor cells in a substrate, each cell comprising

- 5 - first drain/collector regions (D11, D12) at the respective edge of the cell,
- a second drain/collector region (D22) between the first drain/collector regions (D11, D12),
- source/emitter regions (S11-S21, S12-S22) between the respective first drain/collector region (D11, D12) and the second drain/collector region (D22),
- 10 - first gate/base regions (G11, G12) between the respective first drain/collector region (D11, D12) and the source/emitter regions (S11-S21, S12-S22), and
- second gate/base regions (G21, G22) between the source/emitter regions (S11-S21, S12-S22) and the second drain/collector region (D22),
- the first drain/collector regions (D11, D12) of all cells being interconnected to a common
- 15 first drain/collector terminal (VD1),
- the second drain/collector region (D22) of all cells being interconnected to a common second drain/collector terminal (VD2),
- the first gate/base regions (G11, G12) of all cells being interconnected to a common first gate/base terminal (VG1), and
- 20 the second gate/base regions (G21, G22) of all cells being interconnected to a common second gate/base terminal (VG2).



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ABSTRACT

A differential transistor pair comprises a plurality of transistor cells (C3) in a substrate (8). Each cell comprises first drain regions (D11, D12) at the respective edge of the cell, and a second drain region (D22) in between. Source regions (S11-S21, S12-S22) are located between the respective first drain region (D11, D12) and the second drain region (D22). First gate regions (G11, G12) are located between the respective first drain region (D11, D12) and the source regions (S11-S21, S12-S22), and second gate regions (G21, G22) are located between the source regions (S11-S21, S12-S22) and the second drain region (D22). The first drain regions (D11, D12) of all cells are interconnected to a common first drain terminal (VD1), and the second drain region (D22) of all cells are interconnected to a common second drain terminal (VD2). The first gate regions (G11, G12) of all cells are interconnected to a common first gate terminal (VG1), and the second gate regions (G21, G22) of all cells are interconnected to a common second gate terminal (VG2).

Fig. 2 to be published

